FIG. 1

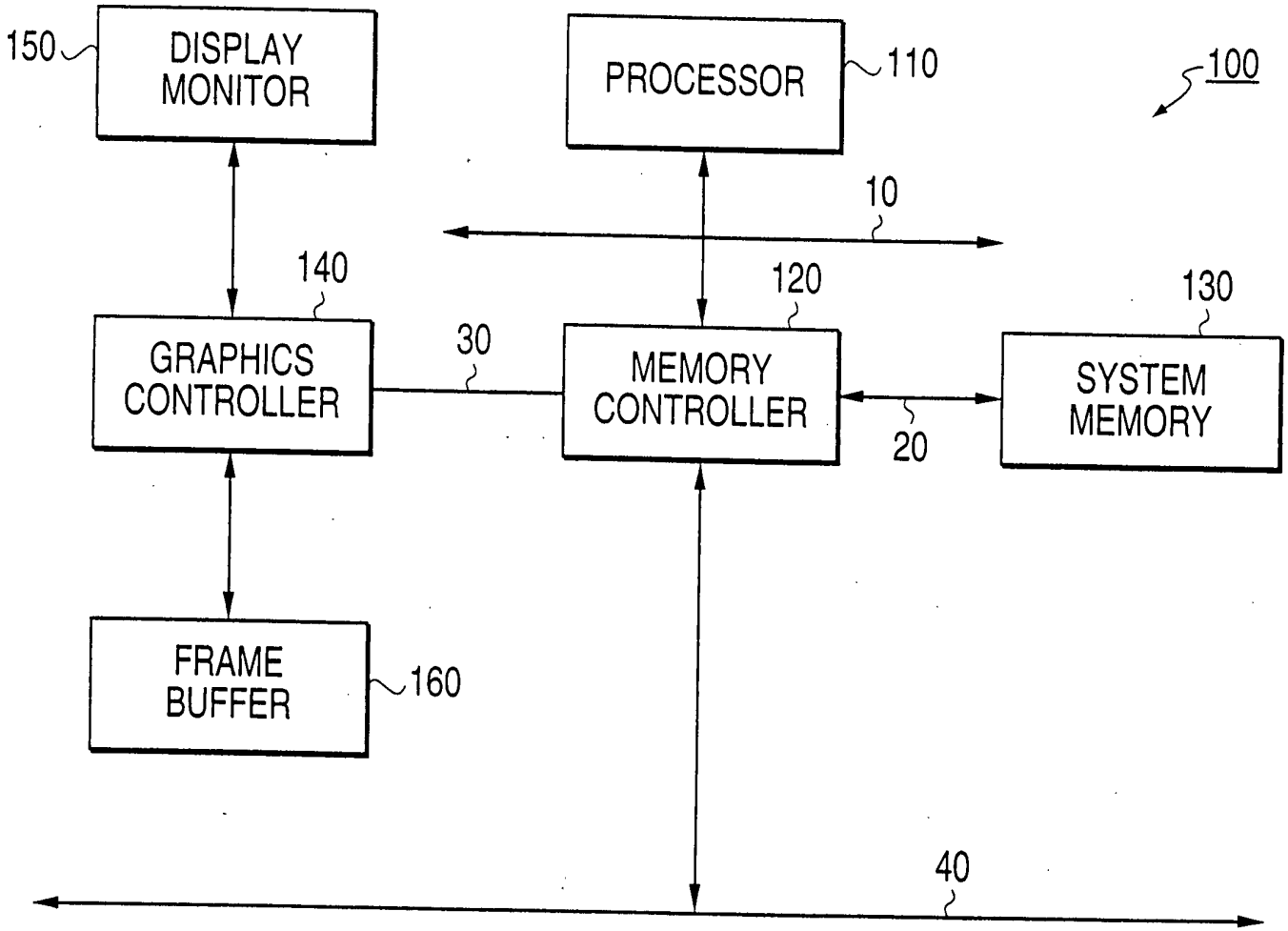
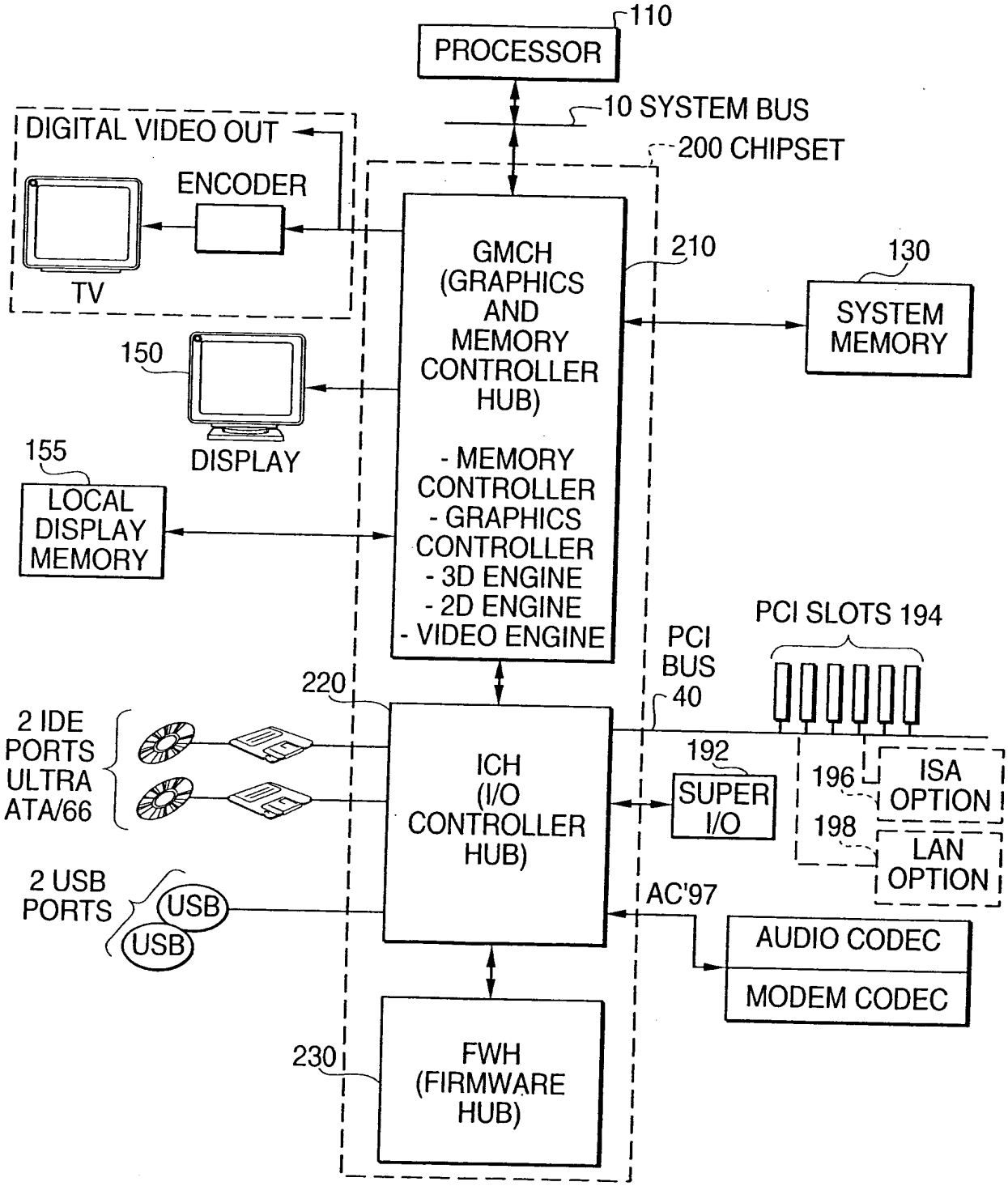

150
DISPLAY MONITOR
PROCESSOR
110
100
10
140
120
130
GRAPHICS CONTROLLER
30
MEMORY CONTROLLER
SYSTEM MEMORY
20
FRAME BUFFER
160
40

FIG. 2


110
PROCESSOR
10 SYSTEM BUS
200 CHIPSET
DIGITAL VIDEO OUT
ENCODER
TV
GMCH (GRAPHICS AND MEMORY CONTROLLER HUB)
- MEMORY CONTROLLER
- GRAPHICS CONTROLLER
- 3D ENGINE
- 2D ENGINE
- VIDEO ENGINE
210
130
SYSTEM MEMORY
150
DISPLAY
155
LOCAL DISPLAY MEMORY
PCI SLOTS 194
PCI BUS 40
220
2 IDE PORTS ULTRA ATA/66
ICH (I/O CONTROLLER HUB)
192
SUPER I/O
196
ISA OPTION
198
LAN OPTION
2 USB PORTS
USB
USB
AC'97
AUDIO CODEC
MODEM CODEC
230
FWH (FIRMWARE HUB)

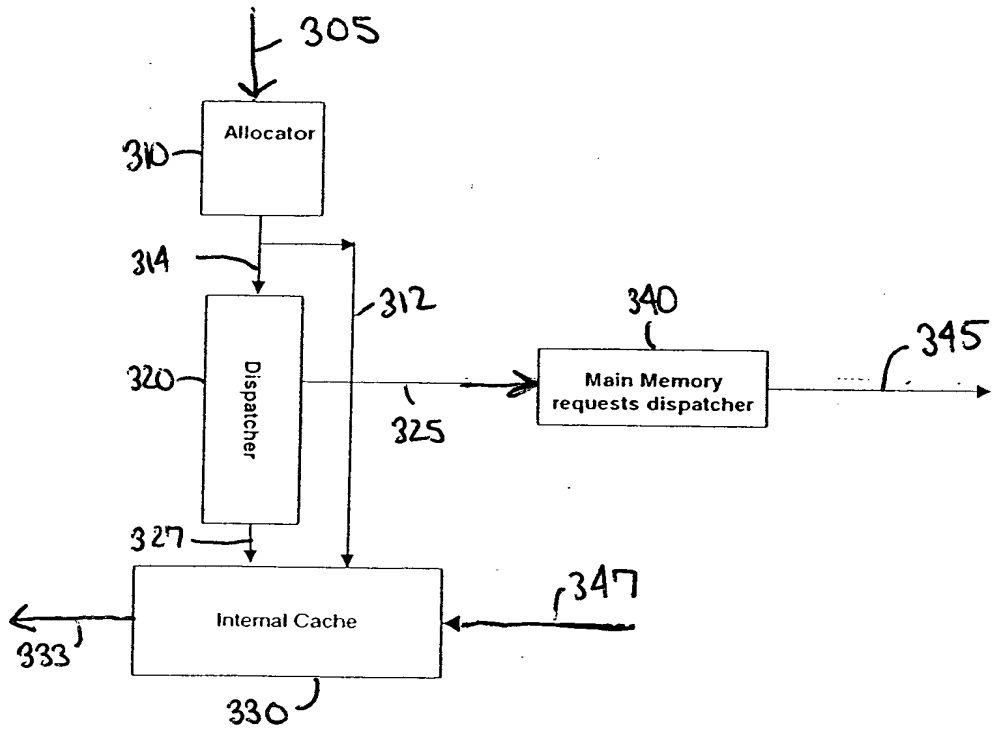

305
Allocator
310
314
312
340
345
320
Dispatcher
Main Memory
requests dispatcher
325
327
347
Internal Cache
333
330

FIG 3

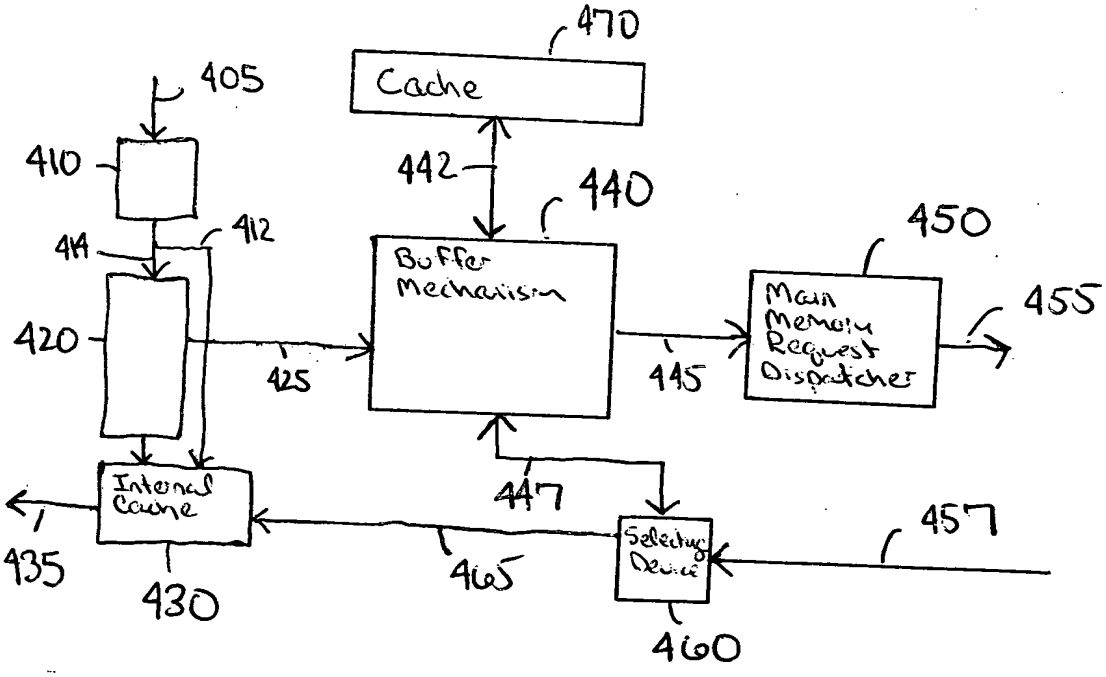

470
Cache
405
410
442
440
450
414
412
Buffer Mechanism
Main Memory Request Dispatcher
455
420
425
445
Internal Cache
447
457
435
465
Selecting Device
430
460

FIG 4

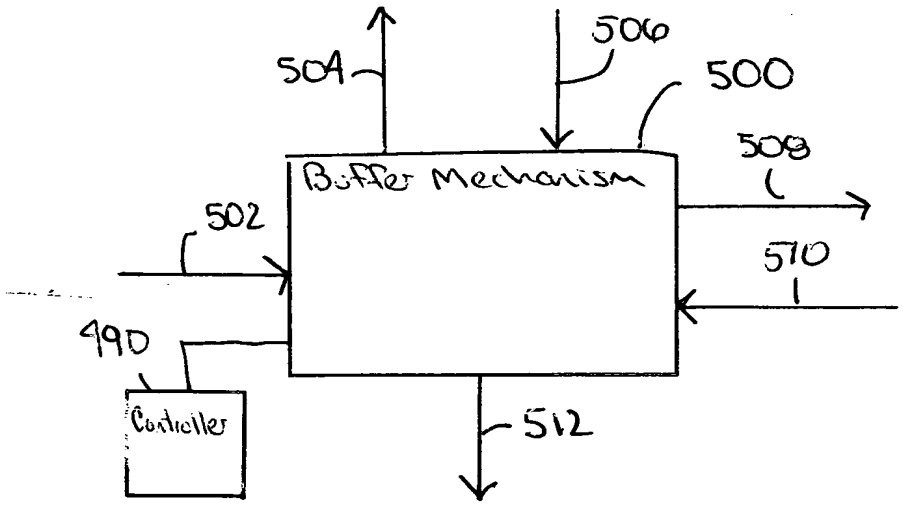


FIG. 5

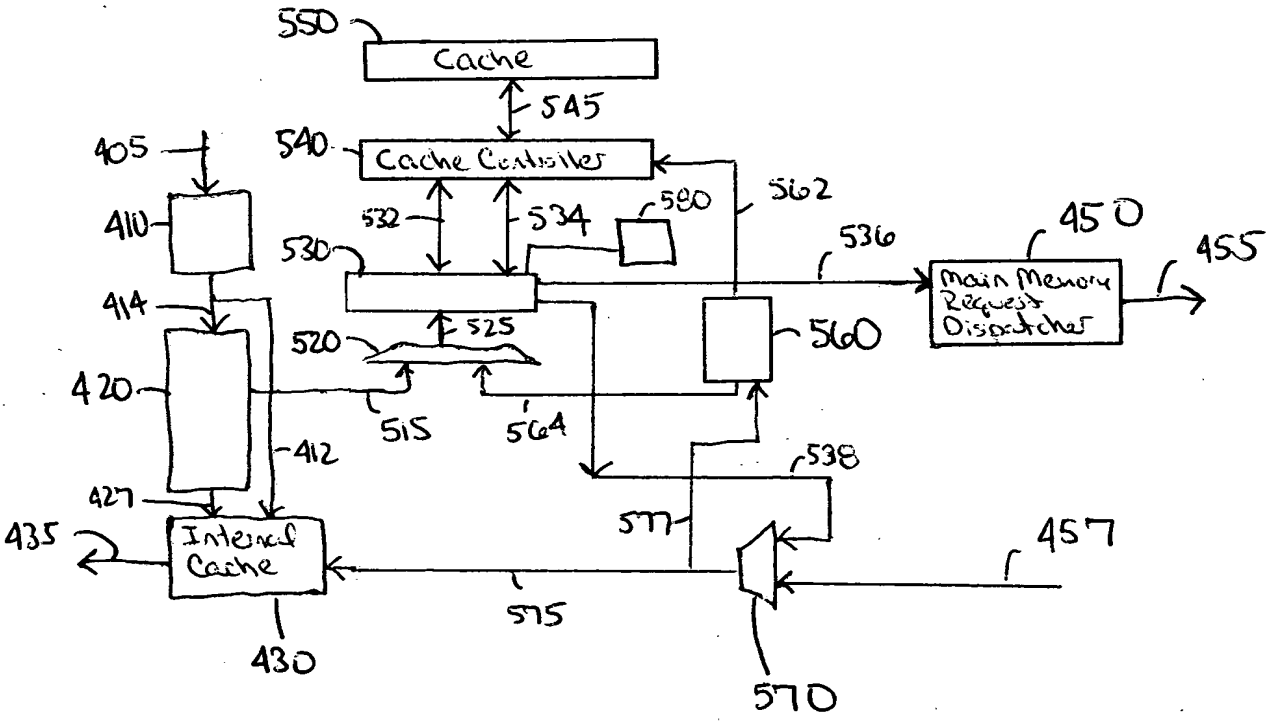

550
Cache
545
405
540
Cache Controller
562
410
532
534
580
450
455
530
536
Main Memory Request Dispatcher
414
525
520
560
420
515
564
412
538
427
577
435
Internal Cache
457
575
430
570

FIG. 6

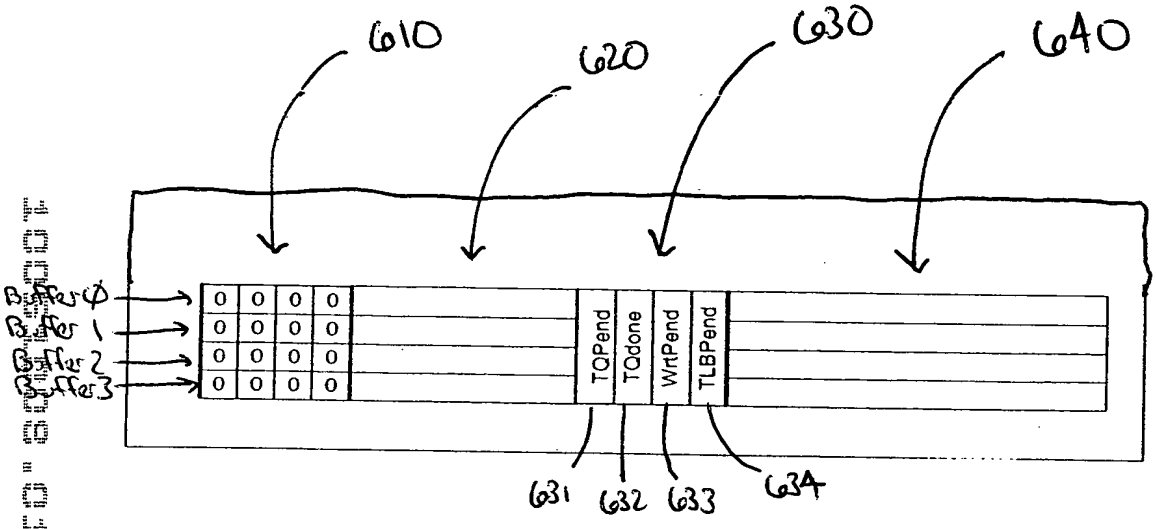

610
620
630
640
Buffer 0
Buffer 1
Buffer 2
Buffer 3
0 0 0 0
0 0 0 0
0 0 0 0
0 0 0 0
TQPend
TQdone
WrtPend
TLBPend
631
632
633
634

FIG 7

FIG 8A

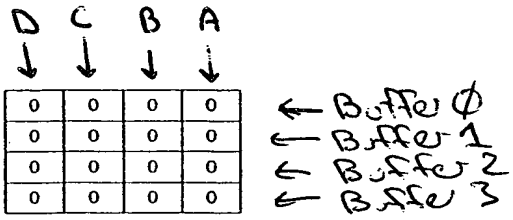


FIG 8B

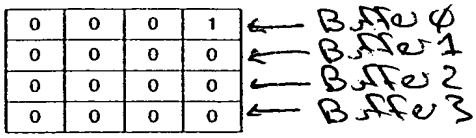


FIG 8C

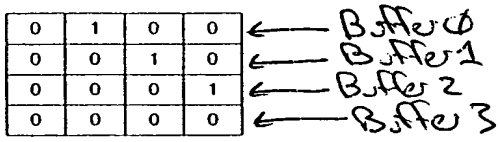


FIG 8D

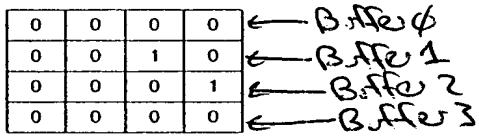


FIG 8E

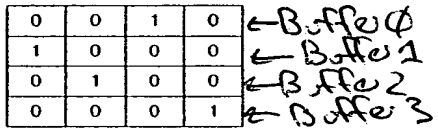


FIG 8F